Your name:

CSE 30341 Operating Systems: Module 3 Exam

OPEN BOOK, OPEN NOTES, CLOSED ELECTRONIC SEARCHES

INDIVIDUAL EFFORT

Duration: 50 minutes.

Choose 6 of 7. I will grade the first six questions that you answer.
Ockham's Razor principles (or Keep It Simple, Stupid: KISS principles) hold. *Make no more assumptions than is needed*. You may write your justification for your answer in the space below. I look at the argument to give partial credit. You can also use these argument to convince me in person that your answer was correct (using only the assumptions and arguments written by you in the answer). Football penalty rules do not apply to his exam, there will be no penalty for you in trying to convince me

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1) A computer with a 32-bit address uses a two-level page table. Virtual addresses are split into a 9-bit top-level page table field, an 11-bit second level page table field and an offset. How large are the pages and how many are there in the address space? (From Tanenbaum)

2) Answer Yes or No: The OS will flush a processes' TLB entries during
   a. Process context switches: _____
   b. Kernel thread context switches: _____
   c. User thread context switches: _____

3) Suppose the hardware supported frames of size *p*. The OS can create a smaller page by safely placing two pages from different processes into the same frame. True or False. Justify.

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4) Consider a paging system with the page table stored in memory. A memory reference takes 200 nanoseconds and 75 percent of all page-table references are found in the TLBs. What is the effective memory reference time? (assume that finding a page-table entry in the TLBs takes zero time, if the entry is in there). (derived from 8.9)

5) What is the purpose of paging the page tables? (Exercise: 8.13)

6) Name one advantage and one disadvantage of a page size 4MB as compared to a size of 4KB.

7) Identify the step that is **not** required during a process context switch from process P1 to P2 in a Pentium based machine:
    a. Store register contents of P1 in its PCB and restore register contents of P2 from its PCB
    b. Flush the TLB caches
    c. Store the current page table from MMU into P1's PCB and restore the page table from P2's PCB into the MMU
    d. Restart the instruction from the current program counter.